

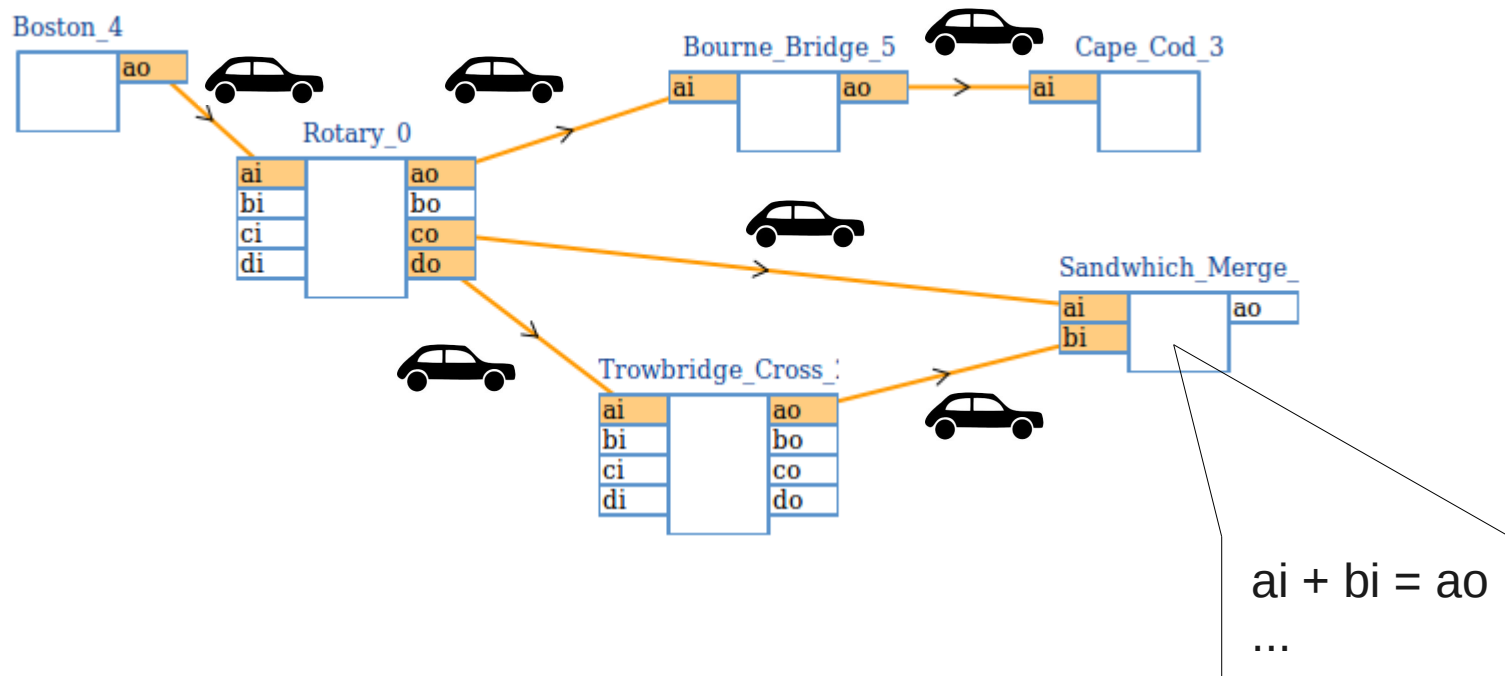
Safe Compositional Equation-based Modeling of Constrained Flow Networks

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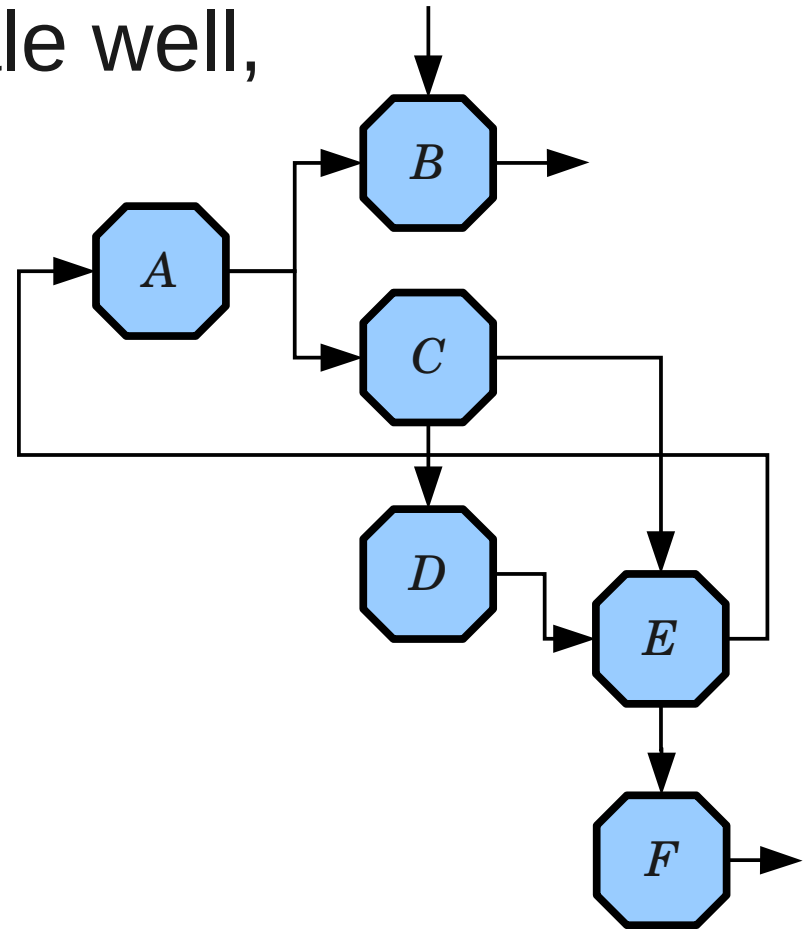
Introduction: Constrained Flow Networks

- Flows between nodes regulated by constraints
- Example domain: Vehicular Road Traffic



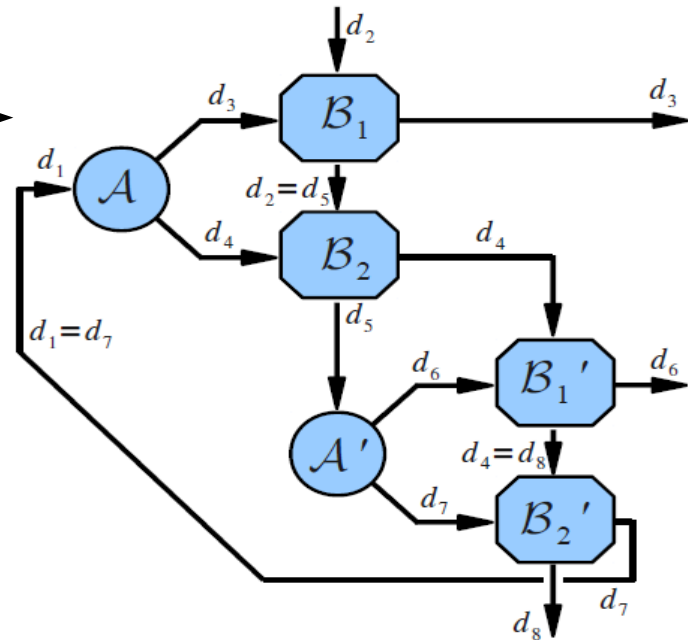
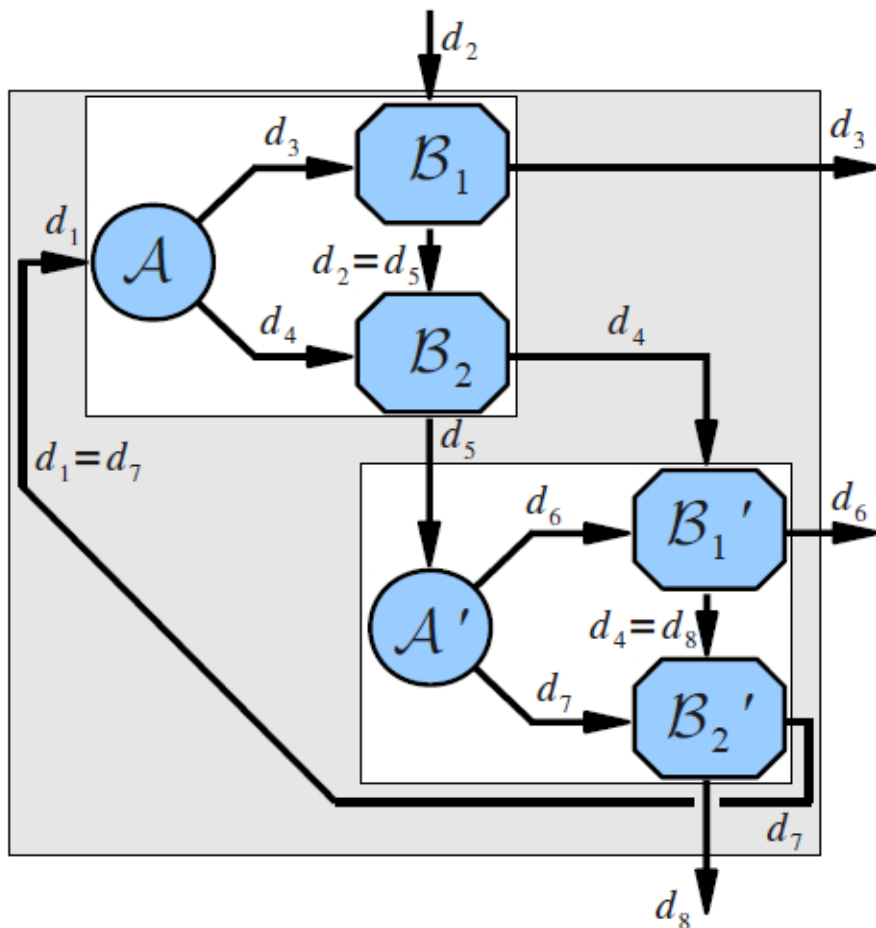
Introduction: NetSketch

- **Problem:** Traditional analysis of constrained flow networks doesn't scale well, cope with unknowns
- **Solution:** NetSketch
 - Lightweight, efficient, scalable modeling and analysis
 - Formalism/DSL
 - Web-based Tool



Introduction: NetSketch

Whole System Analysis →



← Compositional Analysis

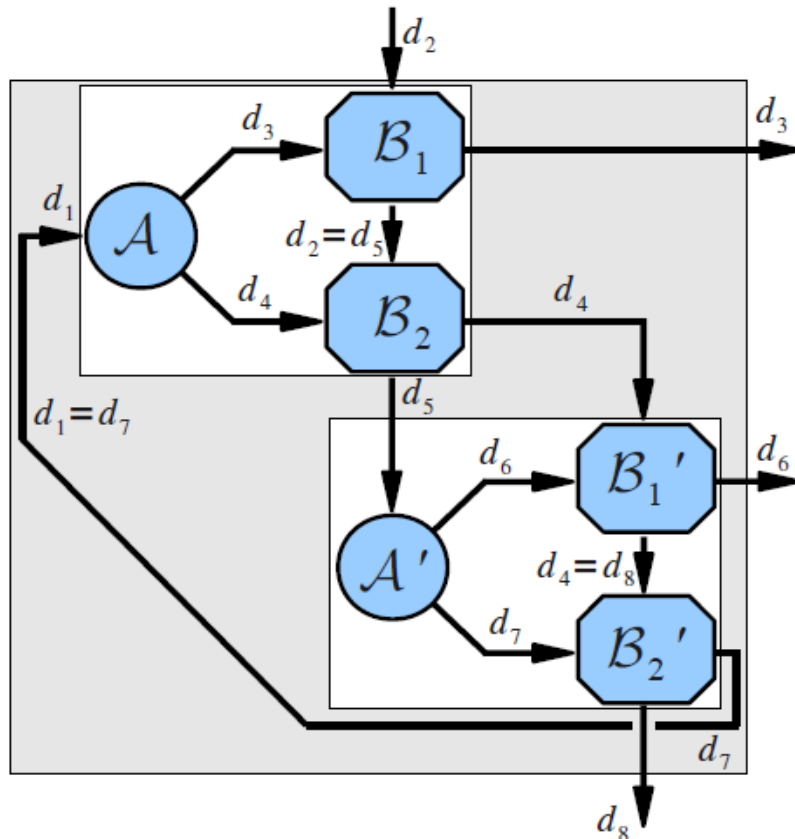
Compositional Analysis via Type Approximations

Traditional Types

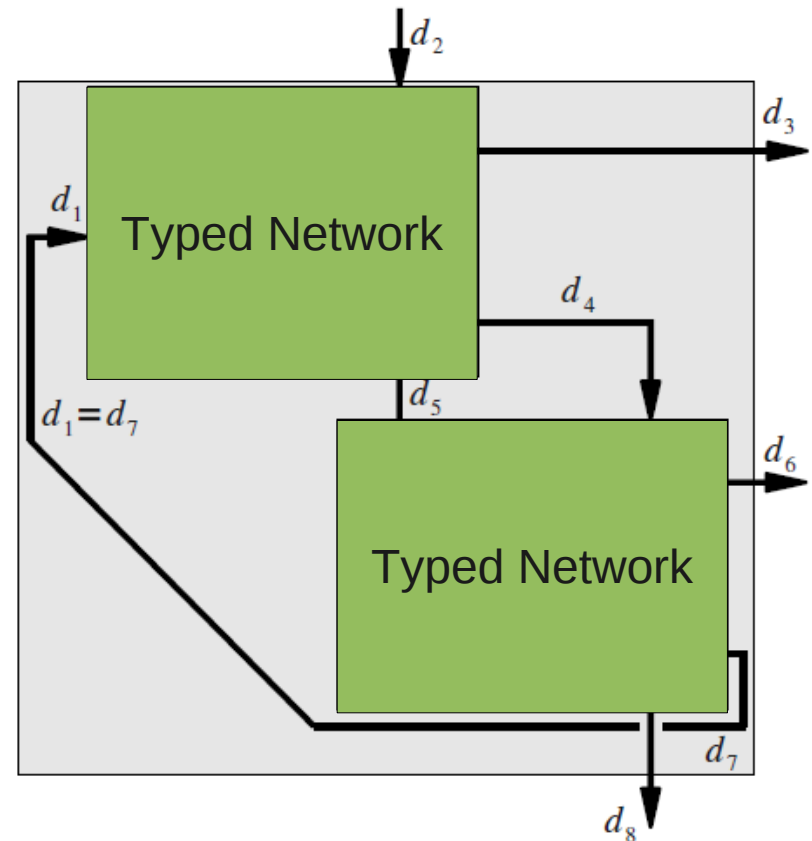
```
int add(int a, int b) {
    return a + b;
}
```

Type system allows the compiler to verify this is safe without knowledge of the exact values or representation of vars

NetSketch Types

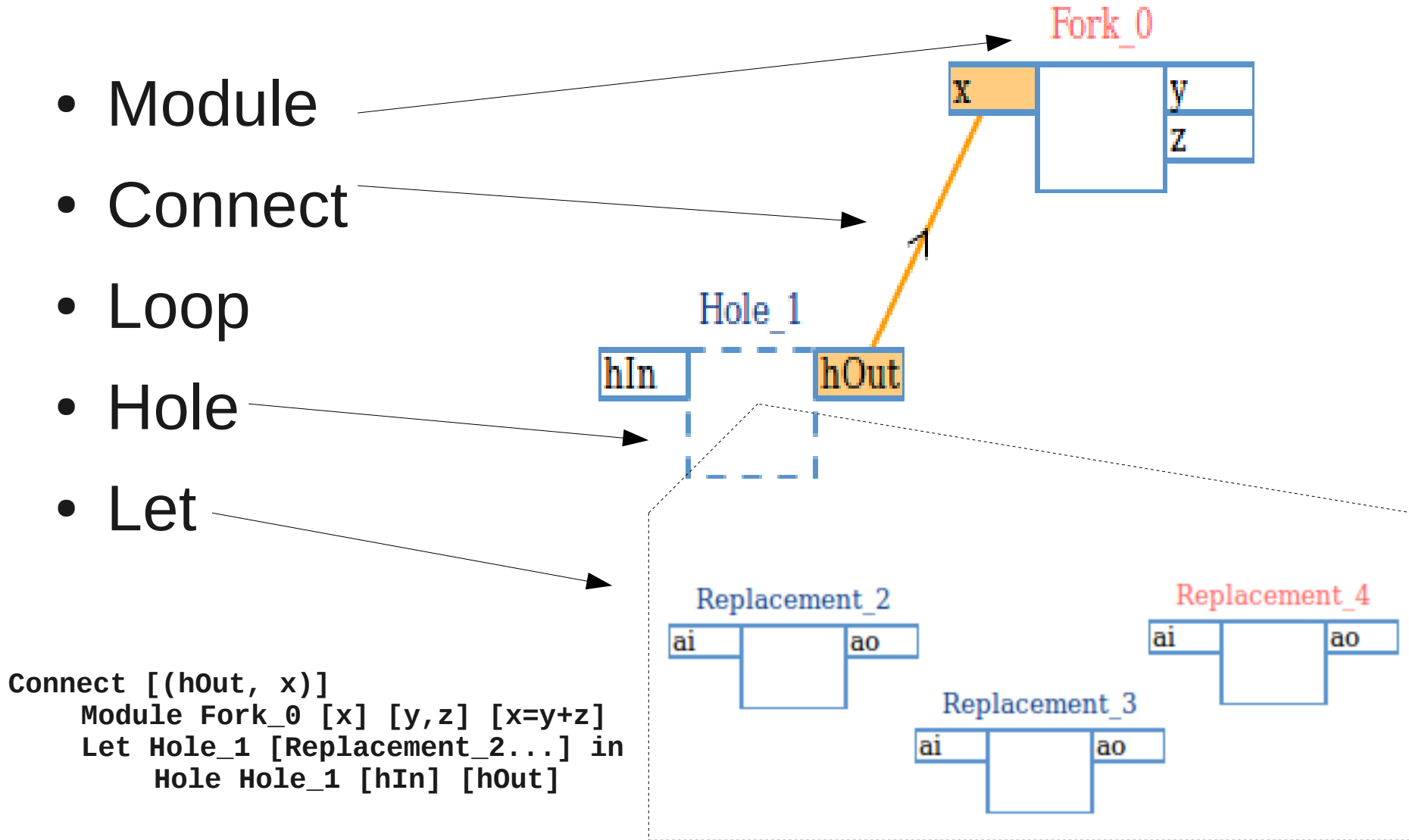


EOOLT 2011



NetSketch DSL

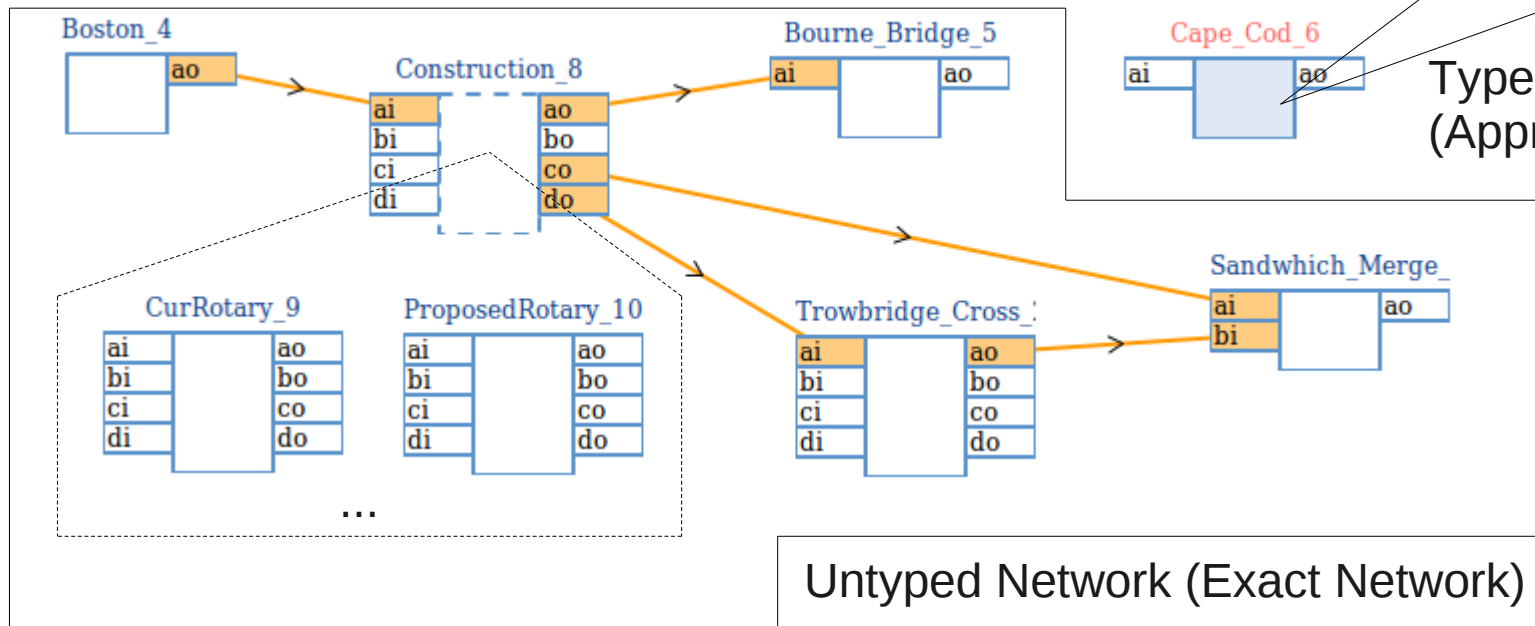
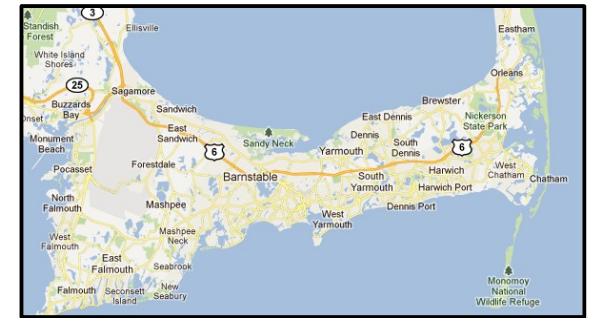
- Module
- Connect
- Loop
- Hole
- Let



Example Model

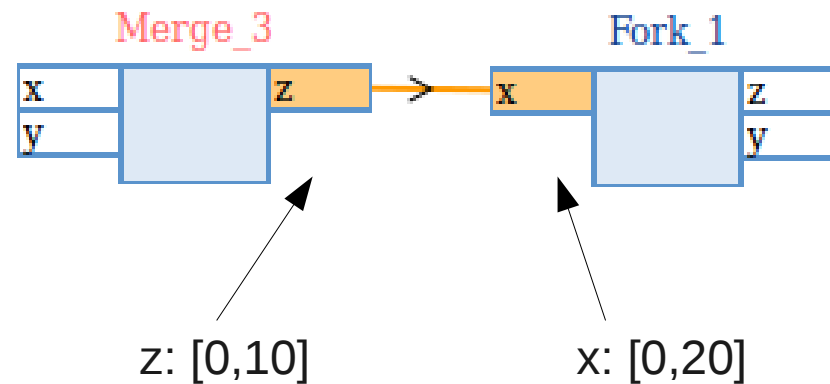
Element	Represents
Boston_4	Module (untyped network)
Construction_8	Hole (untyped network)
CurRotary_9	Replacement (untyped network)
ProposedRotary_10	Replacement (untyped network)
Cap_Code_11	Typed Network

Untyped Network (Exact Network)



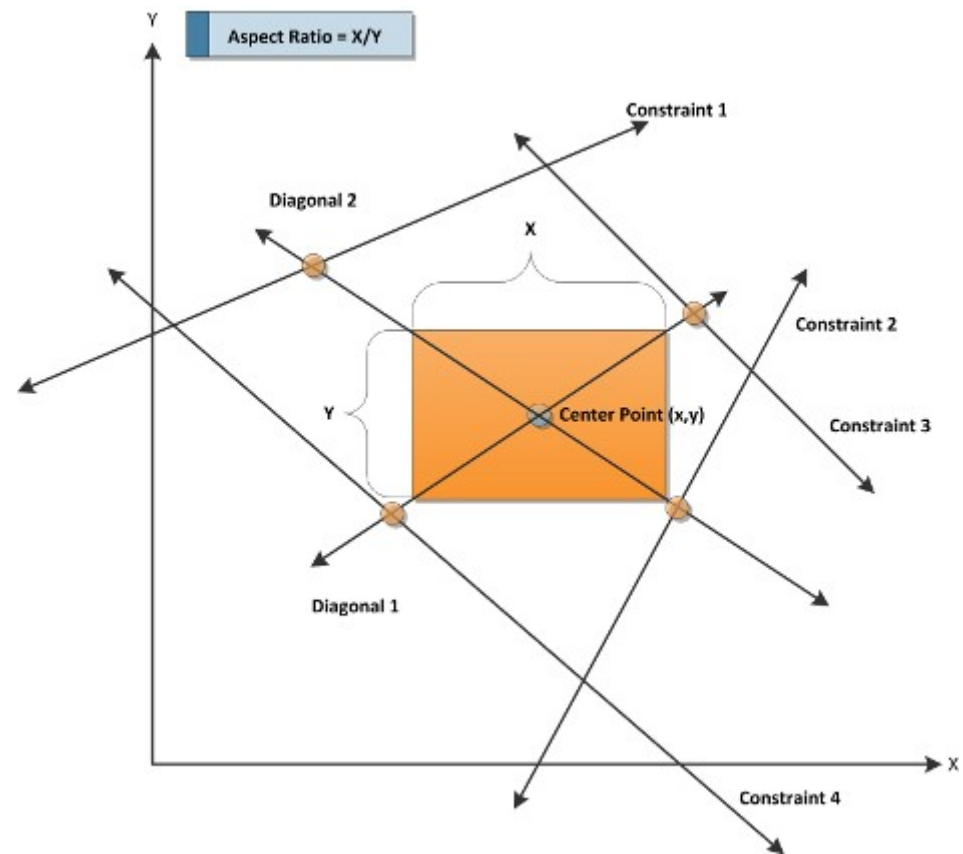
Type System

- Current implementation:
 - Types are open/closed intervals over \mathbb{R}
 - Linear constraints are analyzed to determine:
 - Safe intervals for input ports
 - Safe intervals for output ports



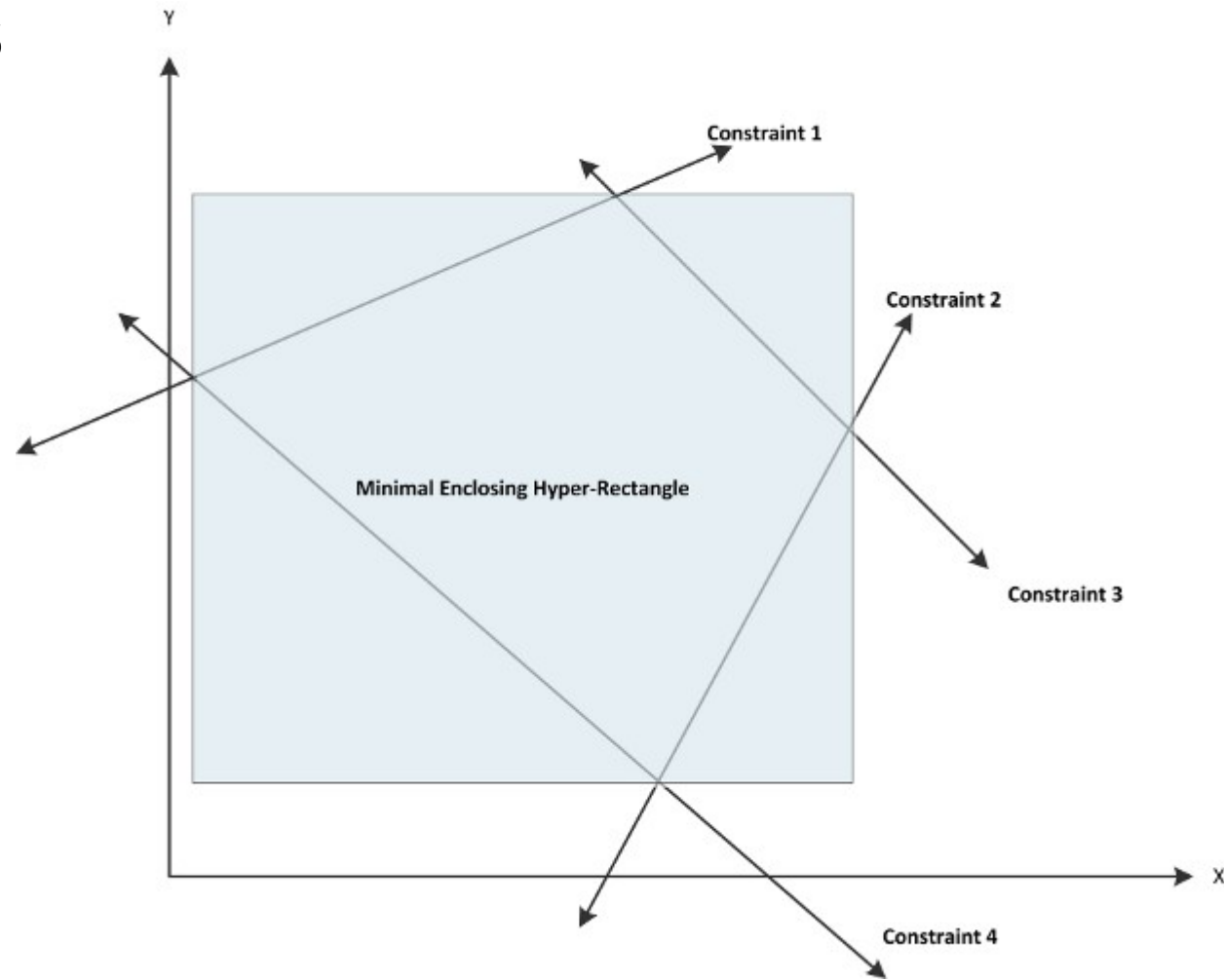
Type Inference: Input Types

- Linear constraints form a convex hull
- Input types approximate the feasible region
- Types derived from maximally enclosed axis-aligned hyperrectangle
- Made unique via:
 - Center point
 - Aspect ratio



Type Inference: Output Types

- Again constraints form convex hull
- Must use maximally *enclosing* hyperrectangle
- Unique without further user input



NetSketch Tool

The screenshot shows the NetSketch Tool interface. The top part displays a circuit diagram with components like CPU_1, CPU_0, CPU_2, CPU_3, Hypervisor_4, Demux_7, VCPU_5, VCPU_6, VCPU_8, Mux_20, AmzLargeSpec_19, and AmzSmallSpec_17. The bottom part shows the properties panel for 'Hypervisor_4'.

Constraints

Constraint
ina+inb=outab
inc=outc
ind=outd

Variables

Variable	Type	Is Bound	Center Coordinate	Aspect Ratio
ina	INPUT	true	0	0
inb	INPUT	true	0	0
inc	INPUT	true	0	0
ind	INPUT	true	0	0
outab	OUTPUT	true	N/A	N/A
outc	OUTPUT	true	N/A	N/A
outd	OUTPUT	true	N/A	N/A

Environment

Key	Value
AlwdVar	.05
VrtOhd	.05

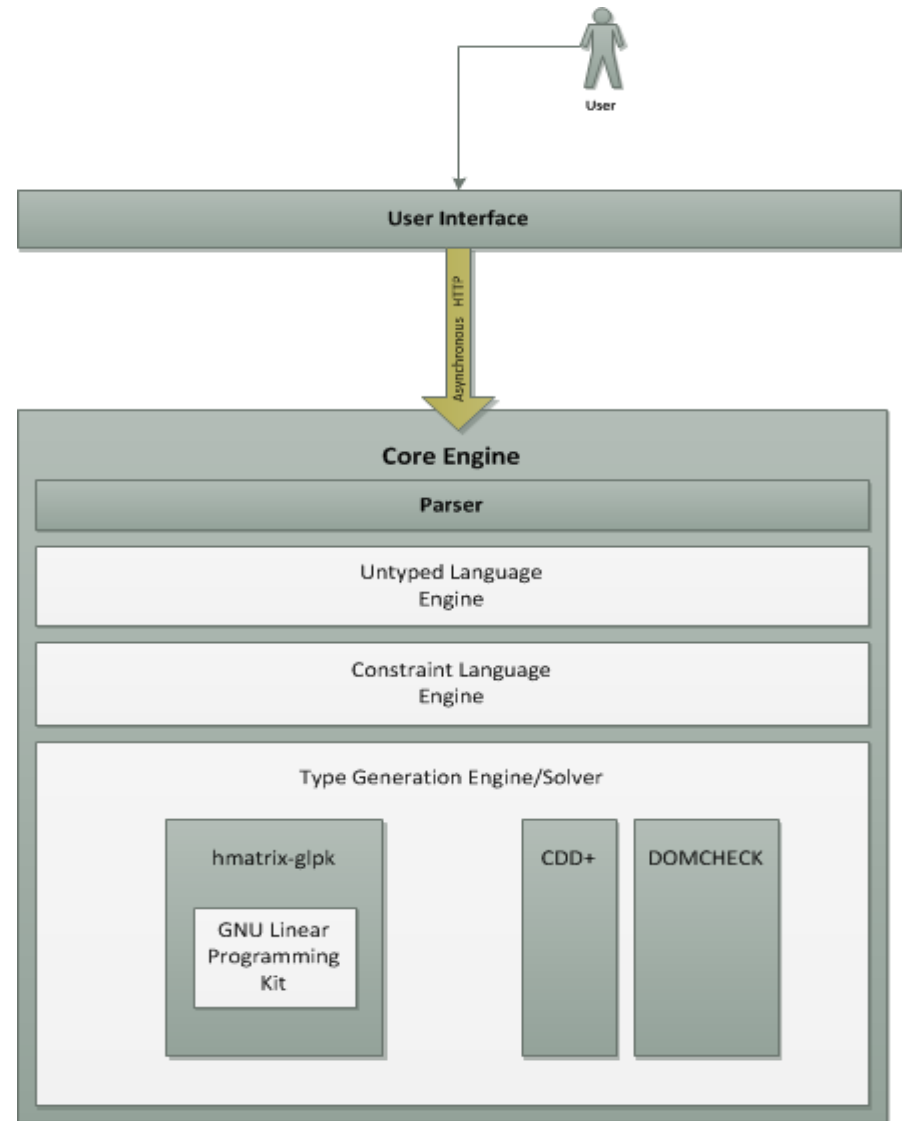
Constraints

Variable Metadata

Canvas

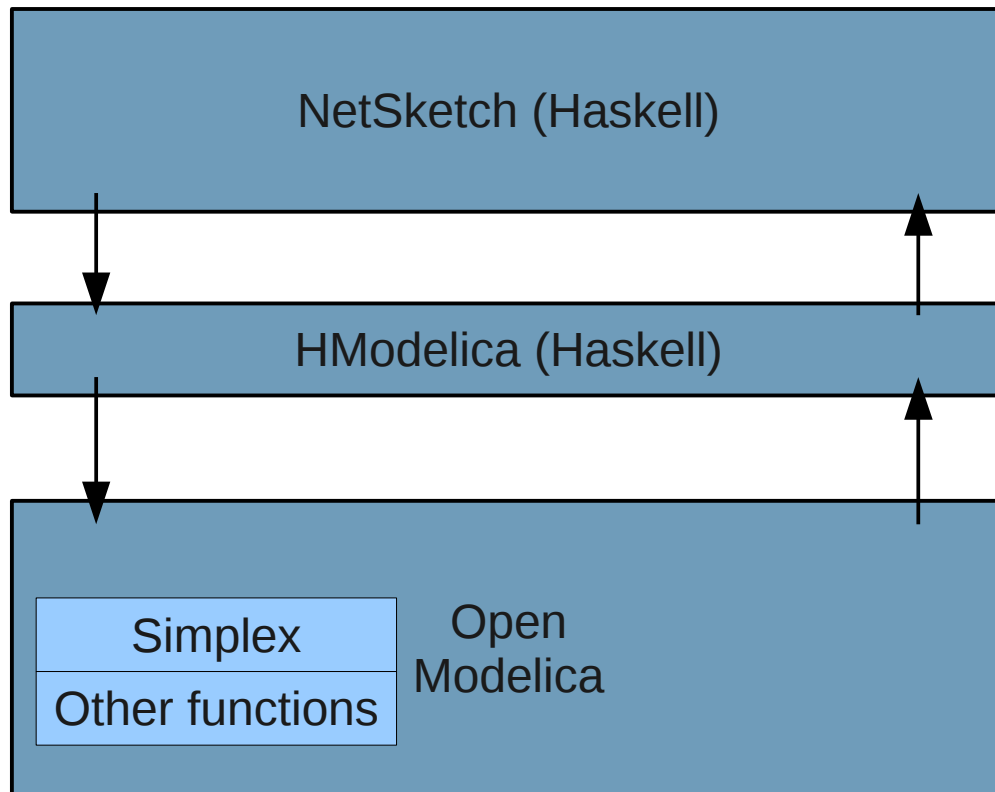
NetSketch Architecture

- Web Based Front End
 - JavaScript
 - HTML
- Server Back End
 - Haskell
 - C
 - C++
- Asynchronous JavaScript and XML (AJAX) based communication

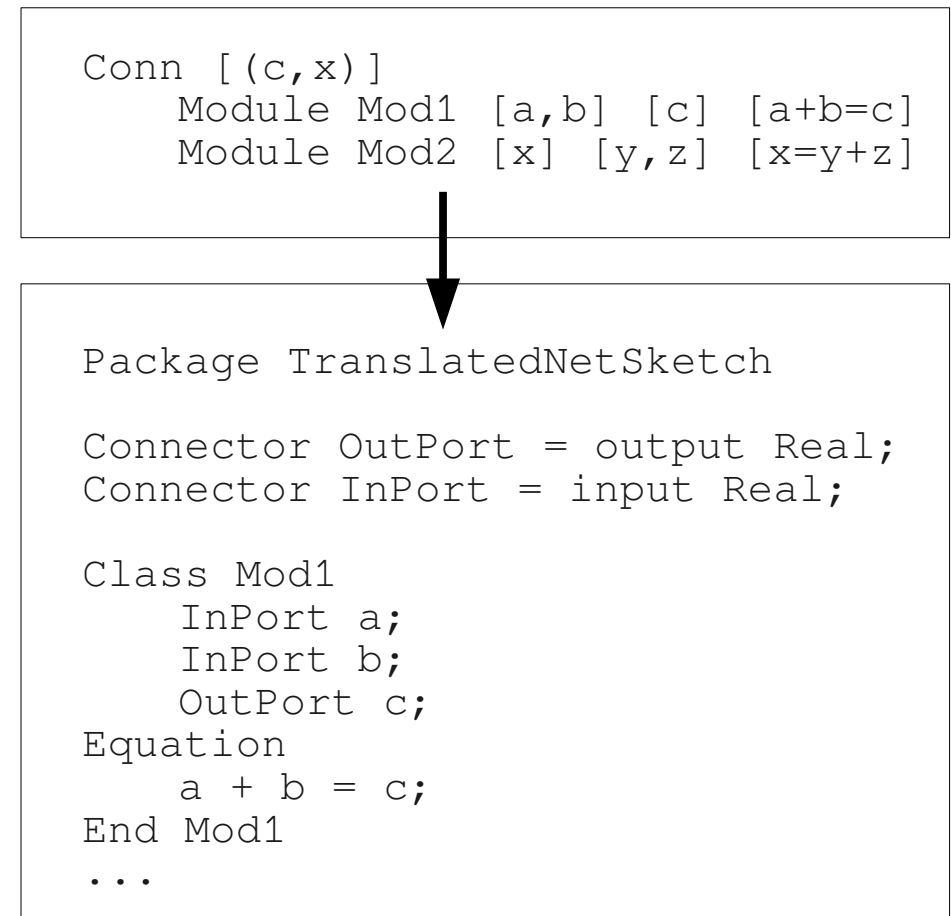


Harnessing Modelica

Computation Platform



Simulation Platform



Current and Future Work

- Constraint and type extensions
 - Adaptive Dynamic Types
 - Variations of constraints
- Tool extensions
 - Bi-directional flow, extended *Let* functionality, internal variables, export to Modelica
- Modelica integration
 - Extend/refine HModelica
 - Modelica -> NetSketch translation

Thank You

More info at: <http://www.cs.bu.edu/groups/ibench>